CLAIMS

1. A method for performing a high stress built-in self-repair for a memory, comprising the operations of:

providing an internal clock signal for use in accessing a memory array, the memory array having access to redundant memory cells during normal operation;

performing a built-in self-test on the memory array using a stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration than each pulse of the internal clock signal;

storing defective memory addresses detected by the built-in self-test in a memory block; and

redirecting memory access operations to the defective memory addresses to redundant memory cells.

2. A method as recited in claim 1, wherein the memory block is a register.

3. A method as recited in claim 1, wherein the internal clock signal is based on required read and write times for memory cells of the memory array.

4. A method as recited in claim 3, wherein the internal clock signal is further based on a margin added to the required read and write times for memory cells of the memory array.

5. A method as recited in claim 4, wherein an amount of optimal margin is derived from expected variations in required read and write times for the memory cells of the memory array due to possible variations in environmental conditions and operating conditions.

6. A method as recited in claim 5, wherein each pulse of the stress clock signal is approximately equal to each pulse of the internal clock signal minus the margin.

7. A method as recited in claim 6, wherein the stress clock signal is not used during normal memory access operations.

8. A method as recited in claim 7, wherein the internal clock signal is used during normal memory access operations.

9. An integrated circuit memory device, comprising:

an internal clock signal for use in accessing a memory array, the memory array having access to redundant memory cells during normal operation;

a stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration than each pulse of the internal clock signal;

a built-in self-test circuit that performs a built-in self-test using the stress clock signal;

storage that stores defective memory addresses detected by the built-in self-test circuit; and

redundant control logic that redirects memory access operations to the defective memory addresses to redundant memory cells.

10. An integrated circuit memory device as recited in claim 9, wherein the internal clock signal is based on required read and write times for memory cells of the memory array.

11. An integrated circuit memory device as recited in claim 10, wherein the internal clock signal is further based on a margin added to the required read and write times for memory cells of the memory array.

12. An integrated circuit memory device as recited in claim 11, wherein an amount of optimal margin is derived from expected variations in required read and write times for the memory cells of the memory array due to possible variations in environmental conditions and operating conditions.

13. An integrated circuit memory device as recited in claim 12, wherein each pulse of the stress clock signal is approximately equal to each pulse of the internal clock signal minus the margin.

14. An integrated circuit memory device as recited in claim 13, wherein the stress clock signal is not used during normal memory access operations, and wherein the internal clock signal is used during normal memory access operations.

15. An integrated circuit memory device as recited in claim 14, the integrated circuit memory device is designed using a generator.

16. A built-in self-repair (BISR) system, comprising:

a memory clock generator capable of generating an internal clock signal and a stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration than each pulse of the internal clock signal;

logic coupled to the memory clock generator, the logic capable of selecting between the internal clock signal and a stress clock signal;

a built-in self-test circuit that performs a built-in self-test using the stress clock signal; and

repair logic that performs soft-repairs of defective memory addresses detected by the built-in self-test circuit.

17. A BISR system as recited in claim 16, wherein the repair logic comprises a register that stores defective memory addresses.

18. A BISR system as recited in claim 17, wherein the repair logic further comprises redundant control logic that redirects memory access operations to the defective memory addresses to redundant memory cells.

19. A BISR system as recited in claim 18, wherein the internal clock signal is based on required read and write times for memory cells of the memory array.

20. A BISR system as recited in claim 19, wherein the internal clock signal is further based on a margin added to the required read and write times for memory cells of the memory array.

21. A BISR system as recited in claim 20, wherein an amount of optimal margin is derived from expected variations in required read and write times for the memory cells of the memory array due to possible variations in environmental conditions and operating conditions.

22. A BISR system as recited in claim 21, wherein each pulse of the stress clock signal is approximately equal to each pulse of the internal clock signal minus the margin.

23. A BISR system as recited in claim 22, wherein the BISR system is designed using a generator.